FlexTrate™: High Interconnect Density Fan-Out Wafer Level Processing for Flexible Bio-compatible Electronics


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Outline

1. UCLA CHIPS – A Brief Introduction
2. New Flexible Device Integration Technology
   2-1. Introduction of “FlexTrate®” based on FOWLP
   2-2. Fine-Pitch Interconnect Formation
   2-3. Process Optimization and Evaluation
3. Summary
4. Acknowledgement
SoCs have been driven by Silicon Scaling

1964 - Transistor SLT module
6 transistors, 4 resistors

2016-7 – IBM POWER 9 Processor fabbed @ Global Foundries
14nm SOI eDRAM technology, 650mm²
24 cores and 120MB of on-chip eDRAM memory
8 billion transistors, 17 wiring levels !!

Packaging has scaled modestly

Interconnect density & transistor performance are both important

CHIPS Framework

Integration
A processing facility for Interconnect Fabric (IF) & assembly

Materials
- Fine Pitch Interconnect
- Substrate Materials
- Warpage, Stress Flexible Materials
- Thermal solutions
- Materials for Additive Mfg. Reliability

Devices/Components
- Novel switches
- New memory
- MEMS
- Sensors
- Passives, antennae
- Medical devices

Tier 1 Foundry Partners
Si, Compound Semis, MEMS, and OSATs

Tier 1 Equipment Partners
New Tool Concepts
Tool Development
Scale-Up

Applications & Architecture
- Heterogeneous Systems
- Approximate Computing
- Cognitive Computing
- Fault Tolerance
- Supply chain Integrity Security
- Memory Subsystems
- Processing in Memory DFT
- Network on Board

Design Infrastructure
- Thermo-Mechanical
- Electrical
- Tools
- Partitioning
- DFT
- Active IF Design

Courtesy IBM
High Performance Flexible systems will require high performance heterogeneous Chips and high interconnect density

Self contained implantable and autonomous electronics has widespread applications

• Depression
• Parkinson’s
• Epilepsy
• And many more

But they do need Hi performance processors, heterogeneous components and innovative power delivery and communication and Fine pitch interconnects on flexible substrates to conform and insert

Fan-out Wafer Level Packaging (FOWLP) – a Quick Tutorial

• Developed by Infineon (now Nanium)
• Practiced by n some form or the other by
  • TSMC
  • Amkor
  • ASE
  • ...
An array of thin small dies with sub-functional blocks

Cross-section

Flexible substrate

An extremely thin large die

Flexible substrate

High stress

An array of thin small dies with sub-functional blocks

Flexible substrate

Low stress

Small dielets embedded in a polymeric film enable bendable and stretchable structure. Thin Si is also flexible, but bending would give serious reliability issues with high stress.

Methodology of FlexTrate®

Based on Fan-Out Wafer-Level Packaging (FOWLP)

High-performance heterogeneous devices/components

FlexTrate® allows for hetero integration with high-performance inorganic single crystal semiconductor devices (Si & GaAs etc.) and much tighter interconnects compared to printed flexible electronics with organic semiconductors in roll-to-roll processing.
A Fabrication Flow of FlexTrate® using Flexible FOWLP Process with a Biocompatible PDMS

1. Temporary adhesive layer formation
2. Multichip flip-chip assembly on 1st handler
3. PDMS supply
4. Compression mold
5. Debonding from the 1st handler
6. Metallization on Si and PDMS
7. Debonding from the 2nd handler

Double Flip Transfer process allows wafer-level processing based on fan-out wafer-level packaging to make fine-pitch interconnects and flexible Si & III-V devices.
Properties of a Biocompatible PDMS (SILASTIC® MDX4-4210 / Dow)

<table>
<thead>
<tr>
<th>Properties</th>
<th>Biocompatible PDMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardness</td>
<td>30 (Shore A)</td>
</tr>
<tr>
<td>Tensile strength</td>
<td>5 (MPa)</td>
</tr>
<tr>
<td>Elongation at break</td>
<td>~500%</td>
</tr>
<tr>
<td>Dielectric constant @ 100kHz</td>
<td>3.0 (3.01@100Hz)</td>
</tr>
<tr>
<td>Dissipation factor @ 100KHz</td>
<td>0.001 (0.0009@100Hz)</td>
</tr>
<tr>
<td>Volume resistivity</td>
<td>2×10¹⁵ (Ω·cm)</td>
</tr>
<tr>
<td>CTE</td>
<td>~300 (ppm/K)</td>
</tr>
<tr>
<td>Young modulus</td>
<td>0.5 (MPa)</td>
</tr>
<tr>
<td>Tg</td>
<td>-120 (°C)</td>
</tr>
<tr>
<td>Thermal decomposition temp.</td>
<td>200 (°C) or more</td>
</tr>
<tr>
<td>Screening test</td>
<td>Applicable for implantation in the human body for up to 29 days without encapsulation</td>
</tr>
</tbody>
</table>

Comparison of Multi-Die Placement: K&S CtW Flip-Chip Bonder and Capillary Self-Assembly with Liquid Droplets

(a) Pick-and-Place

Advantage: Tight Die-Die placement with ~1 μm overlay tolerance

(b) Tohuku Capillary Self-Assembly

Advantage: High thru’put Batch assembly is possible with 1-2 μm alignment accuracy
A Surface Profile of Multi-Dies Placed on the 1st Temporary Adhesive on the 1st Si Handler

There is very small die tilt. The maximum height difference among the Si dies is approximately 1.5 µm, similar to the dielet TTV values.

Curing Temperature impact on Final Topography

The height gap is gradually reduced with the decrease in curing temperature.
Reducing First Adhesive Thickness and PDMS curing temperature

*Height difference
A: Between Si
B: Between Si & PDMS

Curing at 40°C

Curing at 25°C

Thinner adhesive layer (10µm) can further reduce the height gap down to 1µm

Summary of final dielet co-planarity studies

- The height gap is gradually reduced with the decrease in curing temperature
- Thinner adhesive layer (10µm) can further reduce the height gap down to <1µm
Water Contact Angle Shift as a Function of Surface Modification Time with UV/O₃, and their Adhesion Properties

By using UV/O₃ treatment, the water contact angle is dramatically decreased, and consequently, the surface is rendered highly hydrophilic.

Fine wiring formation on Si dielets & PDMS: Line Width Meas.

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**Fine wiring formation on Si dielets & PDMS: Line Width Meas.**

- **Au wirings**: Measured width: 18um, Design: 20um
- **Stress buffer layer on PDMS**: Measured width: 18um, Design: 20um
- **Si**: Measured width: 18um, Design: 20um

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**CHIPS**
An Optical Images of 10-µm-pitch Ti/Au Wirings Formed on Si/PDMS at the Wafer-Level

Fine-pitch (pitch: 10µm) wirings are successfully formed on PDMS.

An Optical Images of 8-µm-pitch Ti/Au Wirings Formed on Si/PDMS at the Wafer-Level

Fine-pitch (pitch: 8µm) wirings are successfully formed on PDMS.
Wafer Warpage

625 (25 by 25) Si dielets embedded in PDMS

Typical FOWLP shows serious wafer bow beyond 1mm. This flexible FOWLP technology with PDMS can significantly reduce the thermomechanical stress due to the low glass transition temperature Tg of the PDMS.

Electrical Property of Fine Wirings on FlexTrate®

Theoretical resistance: 122 Ω
@ 18µm(w), 10mm(l), 100nm(t)
(Au: 2.21x10⁻⁸ Ω·m)
Electrical Property before/after Removal & Bending

Before removal & bending
Ave. 134 Ω

After removal & bending
Ave. 148 Ω

~10% increase

Theoretical resistance:
50 Ω
@8µm(w),
1.8mm(l),
100nm(t)
(Au: 2.21x10^-8 Ω·m)

PDMS
1.8mm
Metal rod
Curvature radius:
2.5mm

The flexible substrate FlexTrate® embedding large numbers of small Si dies in the biocompatible PDMS is bendable, wearable and implantable, and can be attached on the curved surfaces such as the human arm or even inserted into the cranium.

625 Si dies embedded in PDMS

625 Si dies embedded in PDMS
Summary

• FlexTrate™ is introduced as a hi-performance wafer-level fan-out process on flexible moulded substrates
  – Biocompatible if needed
  – Heterogeneous integration of high performance dielets including MEMS and sensors, passives, coils, antennae, batteries, supercaps…..
  – High density Interconnects
  – Embedded Fluidic interconnects
• Tight lithographic alignment of dies and wiring
• Mechanical /electrical testing in progress

Acknowledgements

• DARPA (N00014-16-1-2639 )
• Members of the UCLA CHIPS consortium,
• GINTI, Tohoku University
• Dow Corning for the PDMS materials used in this work
• NITTO for the adhesives
• MetrospeX LLC and Cyber Technologies for analytic services